| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/924,272 | METZGEN, PAUL | |
| | Examiner | Art Unit | |
| | Tuan A. Vu | 2193 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/3/006*.

2. ☒ The allowed claim(s) is/are *1-4, 6-8, 10-11, 13-17, 19, 21-23, 25-27(renum 1-21)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *5/23/06* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## DETAILED ACTION

1. This action is responsive to the Applicant's response filed 4/3/2006.

As indicated in Applicant's response, claims 1, 4, 6-7, 10-11, 13, 16-17, 19, 21-23, 25-27 have been amended. Claims 1-4, 6-8, 10-11, 13-17, 19, 21-23, 25-27 are pending in the office action.

## EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Michael Chasan, Reg. # 54026 on 5/23/06.

The application has been amended as follows.

In the CLAIMS,

**Claim 1**:

A method for generating hardware configuration data directly from high-level software ~~constructs~~ programming code and configuring a programmable logic resource with the hardware configuration data, the method comprising:

parsing high-level software programming code transparent with regard to hardware to locate at least one expression in the programming code that is used more than once in the program;

compiling hardware configuration data directly from the high-level software programming code, wherein the-hardware configuration data is configured to:

use a single set of hardware resources to implement the at least one expression,

generate a control flow in the hardware, wherein the control flow indicates a status for a block and the status indicates a capability for speculation,

couple ~~an~~ a hardware operation input environment to the block that carries information into the block, and

couple ~~an~~ a hardware operation output environment to the block that carries information out of the block, and

configuring the programmable logic resource with the hardware configuration data, wherein the programmable logic resource is configured to make run-time decisions regarding executing the block at least partially based on the control flow, and to select hardware instances that will have access to the single set of hardware resources.

**Claim 27**:

A method for generating hardware configuration data directly from high-level software ~~constructs~~ programming code and configuring a programmable logic resource with the hardware configuration data, the method comprising:

parsing high-level software ~~constructs~~ programming code that ~~are~~ is transparent with regard to hardware to locate at least one expression in the programming code that is used more than once in the program;

compiling hardware configuration data directly from the high-level software ~~constructs~~ programming code, wherein the ~~compiling comprises~~ hardware configuration data is configured to:

use a single set of hardware resources to implement the at least one expression,

generate a control flow in the hardware, wherein the control flow indicates a status for a block and the status indicates a capability for speculation, and

~~mapping a~~ map at least one software construct variable into a hardware construct comprising a set of wires, wherein one of the wires indicates whether the variable has been computed and the remainder of the wires indicate a value of the variable; and

configuring a programmable logic resource with the hardware configuration data, wherein the programmable logic resource is configured to make run-time decisions regarding executing the block at least partially based on the control flow, and to select hardware instances that will have access to the single set of hardware resources.

***EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE***

3. Claims 1-4, 6-8, 10-11, 13-17, 19, 21-23, 25-27 are allowed.

The following is an examiner's statement of reasons for allowance.

The prior art taken separately or jointly does not suggest or teach the following features.

A method for generating hardware configuration data directly from high-level software programming code and configuring a programmable logic resource with hardware configuration data, comprising (i) parsing high-level programming code to locate expression in the code that is used more than once in the program; compiling hardware configuration data by using a single set of hardware resources to implement the one expression; (ii) generating a control flow in the

hardware to indicate a speculation capability for a block execution with a control status, and coupling hardware operation input/output to carry information in/out of the block; and (iii) configuring the programmable logic resource with hardware configuration data using this configuration data to make run-time decisions regarding executing the block at least partially based on the control flow, and to select hardware instances that will have access to the single set of hardware resources, as recited in **claim 1**;

OR

a method as recited above comprising the parsing as in (i); and further including (iv) mapping at least one software variable into a hardware construct comprising a set of wires, wherein one of the wires indicates whether the variable has been computed and the remainder of the wires indicate a value of the variable; and configuring the programmable logic resource with hardware configuration data as in (iii); as recited in **claim 27**.

**Panchul**, USPN: 6,226,776, discloses mapping high-level programming code like HDL into register translation language using hardware constructs like a set of wires, one of which is to control the flow of the rest of wired data into a hardware block; but fails to teach or disclose compiling as recited in (i) directly from the high level program such that it uses a single set of hardware resources following the identifying of expressions used more than once; and based on the control flow and speculation status for a block execution (ii), making runtime selection of hardware instances based on the control flow as in (iii) of hardware operation that will access that single set of hardware resources as in (i); nor does Killian teach or suggest the compilation as in (i) to map directly program variable into a set of hardware wires as in (iv) in order to make runtime selection based on the control status of the block as in (ii) and (iii).

**Killian**, USPN: 6,477, 683, teaches hardware definition language and mapping into intermediate language like JTAG to implement wires of hardware runtime; but fails to teach or suggest identifying of program expressions used more than once, and configure a programmable hardware resource using a single set of hardware resources from the direct configuration as in (i) and (ii); and making runtime decisions to select hardware instances as in (iii) to access that set of hardware resources from (i); partially based on the control flow speculation status of (ii), or the wire mapping in (iv) for configuring the programmable logic resource.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)272-3719.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 ( for non-official correspondence – please consult Examiner before using) or 571-273-8300 ( for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT
May 25, 2006

WEI ZHEN
SUPERVISORY PATENT EXAMINER